REMARKS

Claims 12-23 are pending. The specification and claims 12-14 and 16 are amended and claims 1 and 3-11 are canceled without prejudice or disclaimer. New claims 18-23 are added. A marked-up version showing the changes to the specification and claims made by the present amendment is attached hereto as **"Version with markings to show changes made."**

Prompt and favorable action is earnestly solicited.

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees which may be due with respect to this paper, may be charged to Deposit Account No. 01-2340.

Respectfully submitted,

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Attachment: Version with markings to show changes made

VERSION WITH MARKINGS TO SHOW CHANGES MADE
DIVISIONAL OF (09/161,828)

IN THE SPECIFICATION:

The specification has been amended as follows:

Paragraph beginning at page 6, line 11 has been amended as follows:

As shown in Fig. 1, a first aspect of the present invention is a device of a semiconductor device, which comprises: a semiconductor substrate of a ~~firstconduction~~ first conduction type; a drain layer of the first conduction type and formed on a surface layer of the semiconductor substrate; a gate insulating film formed in a partial region on the drain layer; a gate electrode formed on the gate insulating film; an insulating film formed on the gate electrode; a side wall insulator formed on side walls of the gate insulating film, the gate electrode, and the insulating film; a recess formed on the drain layer and in a region other than a region where the gate electrode and the side wall insulator are formed; a channel layer of an opposite conduction type and formed in a range from the region where the recess is formed to a vicinity of the region where the gate electrode is formed; a source region layer of the one conduction type and formed on the channel layer in a region outside the recess; and a wiring layer formed to cover the channel layer which is exposed through the recess, the side wall insulator, and the insulating film.

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IN THE CLAIMS:

Claims 12-14 and 16 have been amended as follows:

12. (Amended) A method of fabricating a semiconductor device, comprising the steps of:

forming a drain layer of a first conduction type on a surface of a semiconductor substrate of the first conduction type;

forming a first insulating film on said drain layer;

forming a first conductive layer on said first insulating film;

forming a second insulating film on said first conductive layer;

patterning said second insulating film, said first conductive layer, and said first insulating film, to form a gate insulating film from said first insulating film, and a gate electrode from said first conductive layer;

implanting an impurity of a second conduction type opposite to the first conduction type into a surface of said drain layer with using said gate electrode as a mask, thereby forming a channel region of the second conduction type;

implanting an impurity of the first conduction type into said channel region with using said gate electrode as a mask, thereby forming ~~a~~ an impurity region of the first conduction type;

forming a third insulating film so as to cover a surface of the

impurity region, side walls of said gate insulating film, said gate electrode, and said second insulating film, and an upper face of said second insulating film;

etching back said third insulating film to form a side wall insulator ~~consisting~~ of said third insulating film, by remaining said third insulating film selectively on side walls of said gate insulating film, said gate electrode, and said second insulating film;

etching the impurity region to form a recess so as to penetrate the impurity region, thereby forming a source region ~~consisting~~ of the impurity region; and

forming a second conductive layer on an entire surface, and patterning said second conductive layer, thereby forming a wiring layer.

13. (Amended) The method of fabricating a semiconductor device, according to the claim 12, ~~wherein~~ further comprising a step of:

introducing an impurity of the second conduction type into the bottom of the recess to form a body contact region of the second conduction after etching the impurity region prior to forming a second conductive layer.

14. (Amended) The method of fabricating a semiconductor device, according to the claim 12, wherein the etching step comprises the steps of:

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forming a mask pattern having an opening located in a center of the ~~source~~ impurity region and cover an entire surface except for the opening before etching the impurity region;

etching the impurity region by using the mask pattern to form a recess ~~shallower than the exposed surface of the impurity region so as to penetrate~~ deeper than the impurity region, thereby forming a source region of the impurity region remained; and

introducing an impurity of the second conduction type into the bottom of the recess to form a body contact region of the second conduction type.

16. (Amended) A method of fabricating a semiconductor device, comprising the steps of:

forming a drain layer of a first conduction type on a surface of a semiconductor substrate of the first conduction type;

introducing an impurity of a second conduction type opposite to the first conduction type into an entire surface of said drain layer, thereby forming a channel layer;

forming a trench so as to penetrate said channel layer and reach said drain layer using a first mask;

forming a first insulating film on an inner wall of said trench and a

surface of said channel layer;

forming a conductive layer on said first insulating film;

forming a second insulating film on said conductive layer;

patterning said second insulating film, said conductive layer, and said first insulating film with using a same second mask, to form a gate insulating film of said first insulating film, and a gate electrode of said conductive layer;

implanting an impurity of the first conduction type into a surface of said channel layer with using said gate electrode as a mask, thereby forming a impurity region of the first conduction type;

forming a third insulating film on an entire surface;

etching back said third insulating film to form a side wall insulator which covers side walls of said gate insulating film, said gate electrode, and said first insulating film;

forming a third mask having an opening located in a center of the ~~source~~ impurity region and cover an entire surface except for the opening, before etching the impurity region;

etching the impurity region by using the third mask to form a recess ~~shallower than the exposed surface of the impurity region so as~~ to penetrate the impurity region and reach to the channel region, thereby forming a source region ~~consisting~~ of the impurity region; and

implanting an impurity of the second conduction type into a bottom of said recess, with remaining said third mask, thereby forming a body contact region; and

removing said third mask; and

forming a second conductive layer which covers said source region, said body contact region, said side wall insulator, and said second insulating film, and patterning said second conductive layer by using a fourth mask, thereby forming a wiring layer.